Qualcomm chose Aptix’s System Explorer to speed the design of the Globalstar satellite system based on CDMA technology. Due to the complexity of the system, both the gateway and phone were prototyped. Real-time prototyping enables designers to perform subjective analysis of voice quality transmitted by the system; this is impossible with simulation.

Wayne Wilson
Design Engineer
Qualcomm (San Diego, CA)
You create a high-performance functional model of your System-on-Chip design in our reconfigurable hardware. Our software quickly maps your custom logic to advanced FPGAs, and you combine those with CPUs, DSP, memories and other IP blocks to complete your circuit. We automatically connect all the design blocks under software control. Our System Explorer plug-and-play architecture is flexible and observable to accommodate the requirements of validating and debugging your design. After you build your prototype, our powerful probing and debugging features provide convenient visibility into the function of your circuit. You implement design changes and ECOs rapidly and easily.

**Reconfigurable SoC Prototyping**

- Debug multi-million gate System-on-Chip designs at speeds up to 40 MHz
- Run system software as your ultimate test bench
- Speed up simulation and accelerate regression testing
- Turn multiple design changes in a single day
- Increase capacity to handle tomorrow’s designs with the latest FPGAs

Real-time verification is essential when developing a complex SoC design. By running our design at its full rated speed, we were able to debug and optimize the software and firmware. Our challenge was to see how much better than the standard specification we could get because the results translate into performance that the cell phone user will experience every day. ... Aptix’s System Explorer tool enabled us to improve our design while shortening our development cycle by seven months.

Luis Aldaz
Philips Semiconductors (San Jose, CA)
Aptix has all the tools you need for emulating and debugging your SoC design in reconfigurable hardware. Automated software synthesizes and partitions RTL logic and maps the design to the prototype hardware. A co-emulation interface allows you to accelerate simulation early in the design process. When you are running your design in-circuit and validating it against real-world data, automated hardware probing provides extensive visibility into the behavior of your circuit.

You run and debug system software on the reconfigurable prototype, even before the hardware design is frozen. Your design runs at MHz speeds in a real-world environment, enabling you to verify your design concept and wring out bugs that traditional verification tools could never attempt to find.

“We delivered at-speed hardware to our software design team at least six months earlier in the design cycle. What’s more, we were able to test many more scenarios than could have ever been simulated. But probably most importantly, the first ASIC silicon worked as specified and required no design turn because of any design problems.”

Vince Dugar, Ben Baron and Randy Fout
Storage Technology (Louisville, CO)

Aptix’s Patented Technology Enables Reconfigurable System Prototyping

FPIC® routing chip provides programmable interconnect
Aptix’s proprietary Field Programmable Interconnect Component® implements electronically reconfigurable, bi-directional interconnect. Any pin can be routed to any pin to create bi-directional, multiple-fan-out nets. FPIC diagnostic components implement software-controlled programmable probing interfaces.

Reconfigurable prototyping platform
Aptix’s Field Programmable Circuit Board® architecture combines a prototyping component area with FPIC interconnect chips to create a reconfigurable prototyping platform. The prototyping area is populated with pin sockets in a Type-C universal pattern to accept Aptix FPGA modules and system components. Each pin socket is routed to a pin on an FPIC routing chip. Connections between the prototyping components are implemented by programming the FPIC chips.
Aptix’s block-based verification methodology means fast prototype creation, easy debugging and rapid implementation of incremental design changes. You build up the prototype block-by-block following the hierarchical organization of your design. During validation you quickly locate bugs in the block-based prototype. Logic changes typically are confined to a single FPGA, enabling rapid bug fixes through incremental compilation and download.

**Design Pilot™ Automates Logic Mapping**

Map your high-level designs to FPGA logic with Aptix’s Design Pilot software. Design Pilot automates logic synthesis with encapsulated one-button operation of leading third-party tools. Design Pilot maps your custom logic and soft IP to the target FPGAs with automatic hierarchical block grouping and partitioning. Optional optimization features let you reduce the number of FPGAs, trading off emulation speed for increased logic density. Design Pilot’s intuitive GUI lets you take direct control of logic mapping when desired.

**Explorer 2000™ Automates Prototype Configuration and Debug**

Aptix’s Explorer 2000 software maps your partitioned design into physical components in the prototyping system and automatically establishes top-level interconnect by routing Aptix’s proprietary FPIC® chips. FPGAs implement custom logic while your choice of CPUs, DSPs and memory chips represent hard IP cores and large memories. The prototype is automatically configured to meet the requirements of your SoC design.

After configuring your prototype, Explorer 2000 automates hardware debugging. From your RTL source you designate the thousands of points you want to observe. The software automatically sets up your Agilent logic analyzer for triggering and data capture. RTL cross probing makes analysis of captured waveforms fast and intuitive.
Get More From Your Simulation Environment

Accelerate your simulation environment with Aptix’s co-emulation solution, Expeditor™. This high-speed interface is a key element of Aptix’s block-based verification methodology. Use block-level test benches to verify the prototype mapping of your stable RTL blocks. Then speed up your RTL simulation by running mixed-level simulation using the prototype to offload the simulator in a co-emulation mode of operation. As you move more RTL blocks to hardware, your RTL simulation speeds up 3X-10X. You accelerate your simulation as you build up your prototype block-by-block. Because prototype implementation mirrors the hierarchical organization of your design, you identify and resolve problems quickly and easily. When your last RTL block becomes stable, you integrate all your blocks in hardware, quickly verify them with your system test bench, and you are ready for in-circuit validation of your complete design.

Expeditor has co-emulation interfaces for popular Verilog and VHDL simulators from Cadence, Mentor/MTI and Synopsys. In addition, Expeditor’s C-API interface enables you to link System Explorer to powerful system simulation environments.

Accelerate Regression Testing

As you debug your prototype in-circuit you will find hardware and software bugs you could never find with pure simulation. As you implement design changes you can save days or even weeks of regression test run times by using Expeditor to accelerate regression tests on the prototype at speeds up to 250 kHz. Expeditor returns results to your workstation’s disk drive for analysis with the VirSim debugging tool embedded in the Explorer 2000 software. Run more regression tests in less time to obtain higher design quality and shorter design cycles.

“Emulation’s high speed can help ease the schedule crunch toward the end of the design cycle because the emulation system can run a comprehensive set of regression tests in a few hours. Simulation regression would normally take much longer.”

Alan Singletary
IBM Corporation

“With the Aptix System Explorer, we were able to develop the Globalstar phone system using an incremental methodology resulting in a savings of at least six months.”

Roy Davis
Qualcomm (San Diego, CA)
Observability Speeds Debugging

Software-controlled hardware probing makes debugging fast and easy. The Explorer 2000 GUI makes it easy to specify the nodes, registers and busses you wish to probe. Explorer 2000 automatically routes hardware probes and configures your Agilent logic analyzer. To provide more than 2,000 probes, Design pilot software automatically inserts probe busses into the FPGAs. Form-based selection automates probe changes and incremental routing delivers results in minutes. Once you have captured data from thousands of nodes, RTL cross-probing makes it easy to view the data of interest. In your RTL code view you identify the signals you want to see, then drag your selection to the VirSim waveform viewer to call up the desired data.

Perform System Integration and Debug Embedded Software Before Silicon Tapeout

Run your code on processor silicon as soon as your RTL is completed. System Explorer’s heterogeneous prototyping environment makes it easy to incorporate multiple IP cores. You can mount processor core silicon directly on the prototype in the form of a plug-in prototyping module or you can cable a connection from the prototype to standard processor development systems. Once you are running with the chip in the emulator, the processor and its software are running in a real-world environment for thorough debugging using your choice of software development environments and tools.

You exercise and debug your code in hardware that mirrors the final system or SoC device. Exercising your code at hardware speeds, months before silicon is available, gives you a great leg up on your project schedules and helps you eliminate the software bottleneck from system and chip bring-up. As you debug your system, you have the freedom to implement changes in the optimal manner. Even though you are running at MHz speeds, your SoC design is still fluid with all its custom logic represented in programmable devices. This lets you implement changes in either hardware or software, all through the lengthy chip floorplanning, synthesis, layout and timing closure process.

Aptix ARM7TDMI plug-in module with JTAG connection for software debugging tools.

“The most important benefit derived from the adoption of the System Explorer was the ability to perform real-time verification of the system.”

Joseph L. Ciccone
Lucent Technologies
(Holmdel, NJ)
Nokia made a commitment to create real-time prototypes of all its new mobile phone designs. Prototypes are the only way to validate our algorithms by testing actual voice transmission quality. We adopted the Aptix solution because it provides a productive debug environment while maintaining our objective of real-time verification.

Stelios Podimatis
Member of Technical Staff,
ASIC Engineering, Nokia (San Diego, CA)
The System Explorer MP4CF is optimized for prototyping circuits with wide internal busses and extensive interconnect requirements. The MP4CF architecture provides maximum routing flexibility for prototypes incorporating many FPGAs and only a few fixed-pin prototyping components (such as a CPU or DSP). Use the MP4CF for building high density prototypes of networking and multimedia systems.

On the Aptix system, the highest density FPGAs are combined with existing logic—including analog components—to emulate a complete video CODEC in real-time. The verification of this chip was a success because we were able to achieve real-time prototyping in a very timely manner.

Tony Luan
Engineering Manager, NEC

Prototyping Modules offered by Aptix

1. ARM/7TDMI
2. 1P/2P memory daughter card
3. A/D converter
4. D/A converter
5. 1M x 64 SPI/AMI daughter card
6. Phase-locked loop
7. 8M x 64 SRAM daughter card
8. Xilinx Virtex 2000E with cable connectors
9. Xilinx Virtex 2000E with cable connectors removed to reveal FPGA package
10. Altera FLEX 10K250
11. Xilinx double-density V2000E
Team-based Verification Provides the Ultimate Acceleration of System Integration

Only System Explorer offers multi-million-gate emulation and stand-alone operation in a desktop package. Use the System Explorer development system for interactive prototype build-up and debug. Then build affordable replicate prototypes for distribution to the project software teams. Your software and firmware engineers no longer have to wait for traditional pre-production prototypes before they begin verifying their code. Now they can work in parallel with the hardware developers and eliminate the traditional software integration bottleneck. The hardware and software engineers are able to find the best way to resolve problems uncovered during real-world testing, rather than resorting to awkward, “last-minute” software workarounds.

Exercise Board-level Hardware in Advance of Prototype Silicon

Your system engineers can use the prototype to emulate the SoC device in its system environment and begin exercising interfaces to other digital and analog subsystems while the SoC development is still in progress.

Deliver Additional Prototypes to Remote Teams Working Across Town or Around the World

As the SoC designers integrate new logic and fix bugs on their development system, they instantly upgrade other prototypes by downloading new configurations over corporate LANs or delivering configuration data to remote sites via FTP. Providing reconfigurable prototypes to your teams around the world enables 24-hour engineering.

Make Sure You are Developing the Product Your Customers Really Want

Build an early prototype to demonstrate proof-of-concept and gather customer feedback. Incorporate new customer requirements into your design and validate the results by updating the prototype. Reconfigurable prototyping with Aptix’s System Explorer enables a totally new approach to SoC development and verification.

A key element of the reconfigurable prototyping methodology is the ability to deliver copies of the prototypes to the software and firmware development teams. We were able to deliver prototypes very quickly, thus giving the developers a significant head start on integrating and testing their code. Because the prototype replicates operate in stand-alone mode, the software developers did not need to know any details of the prototypes’ implementation. They merely turned on the power and the prototypes configured themselves with bit streams stored in on-board FLASH memory. As the hardware design evolved, we gave the developers updated data for configuring the FPGAs and interconnect. This enabled us to instantly update all of the prototypes to the latest design configuration, even those being used in remote locations.

Luis Aldaz
CAE Productivity Engineer, HP
Philips Semiconductors (San Jose, CA)

By putting a replicate system on the desk of all the firmware engineers needing to run code against the ASIC, we were able to save 50 days on code development.

Brian Levy
CAE Productivity Engineer, HP
(Vancouver Printer Division)
Aptix understands that your business is developing products that make you more competitive in the marketplace. While advanced tools are a key part of product development, there are times when you need to complement your resources with help from your suppliers. We also recognize the need to provide professional training and on-going maintenance and support for the products we deliver so you can get the most from your investments. For this reason, Aptix offers Consulting services in addition to traditional hardware and software support and maintenance services.

Aptix Consulting Services—Enabled through eSoCverify.com

Aptix’s Consulting Services Group is there to provide assistance when your team is stretched and your schedules are too short. With our eSoCverify.com secure data center, you take advantage of Aptix’s consulting engineers’ years of experience to help you with everything from mapping your design to the prototyping system to developing any custom modules that might be needed to model unique blocks of your design. By leveraging a secured data center to hold your designs and specifications, Aptix consulting engineers can perform your contracted work at our office, minimizing costly billable trips and visits to your location.

Traditional Support and Training Services

Aptix offers software support through our skilled team of application engineers. Assistance is only a phone call away. Problem reports and requests for assistance can be filed across the Internet 24 hours a day, seven days a week. Our skilled professionals will answer your questions quickly and accurately. Through our Software Maintenance programs, you have access to our Hotline and to software updates and maintenance service packs. These on-going product improvements are easily downloaded across the Internet from our FTP site.

To protect your hardware investment, Aptix offers two levels of Hardware Maintenance Agreements: Basic and Premium. Under Basic Maintenance Aptix will repair in our facilities any product defects as a result of defective parts or workmanship that arise from normal usage of the product. Under Aptix Premium Maintenance, Aptix will deliver a loaner or replacement system to keep you up and running while we repair your system.

Our goal is to provide a broad range of products and services to meet your unique project and business needs. Our success is built upon your success, and Aptix will be there with you.

Product Specifications

- Prototyping Capacity:
  - MP3CF: More than 2.5 million ASIC gates and 6 Mbits block memory with Xilinx Virtex V2000E FPGA modules
  - Upgradable with future FPGA modules (Prototyping area of 1,920 pins with programmable interconnect currently supports up to 12 FPGAs)
  - Multi-system configurations available through Aptix Consulting Services
  - MP4CF: More than 3 million ASIC gates and 10 Mbits block memory with Xilinx Virtex V2000E modules
  - Upgradable with future FPGA modules (Prototyping area of 2,880 pins with programmable interconnect currently supports up to 20 FPGAs)
  - Multi-system configurations available through Aptix Consulting Services

- Probe capacity
  - Through probe bus:
    - MP3CF: more than 1,500
    - MP4CF: more than 2,000
  - Triggerable:
    - MP3CF: 192
    - MP4CF: 256

- Off-board I/O to target system:
  - MP3CF:
    - Edge connector: 480
    - Cable connectors: 640 with interleaved grounds
    - Additional off-board I/O available through cable connectors on FPGA prototyping modules
  - MP4CF:
    - Edge connector: 624
    - Additional off-board I/O available through cable connectors on FPGA prototyping modules

- Physical dimensions:
  - Length: 27.17 inches (69.0 cm)
  - Height: 22.00 inches (55.9 cm)
  - Depth: 6.00 inches (15.3 cm)

- Weight:
  - 47 lb (21.3 kg)

- Electrical Requirements:
  - Supply voltage: 100-230V AC auto-ranging, 48 ~ 62 Hz
  - Power consumption: 5A (max), 400W (max)

- Power supplies for prototyping components
  - (10 A max. each):
    - Vcc: 5.0 v
    - V1: 3.3 v
    - V2: variable: 2.4 v ~ 0.9 v
    - V3: variable: 2.4 v ~ 0.9 v

- Configuration
  - Interactive configuration via Ethernet
  - Stand-alone configuration via onboard FLASH memory, stores up to four designs simultaneously

- Self test
  - Power-on self test for system hardware
  - Connectivity self-test for FPGA prototyping modules mounted in system